



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/000,143	10/23/2001	Gauthier Barret	Barret-1	8524

7590

06/16/2005

Duane, Morris & Heckscher, LLP  
Suite 100  
100 College Road West  
Princeton, NJ 08540

EXAMINER

ELMORE, REBA I

ART UNIT

PAPER NUMBER

2187

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/000,143

Applicant(s)

BARRET ET AL.

Examiner

Reba I. Elmore

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 20 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

1. Claims 1-11 are presented for examination. Claim 12 was cancelled by the amendment filed April 20, 2005.

### *SPECIFICATION*

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

3. The objection to the title is *withdrawn* due to the amendment.

4. The objection to the abstract is *withdrawn*.

5. The objection to the summary of the invention is *withdrawn*.

The objection to the specification is *withdrawn*.

6. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *CLAIM OBJECTIONS*

7. The objection to claim 12 is *withdrawn* due to the amendment.

### *35 USC 112, 2nd paragraph*

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claims 1 and 8, which are the independent claims, have a *second auxiliary memory* claimed which is *distinct and separate from the first memory*. The first memory has not been claimed as an auxiliary memory, in fact, a first auxiliary memory is not present in the claims. There is nothing in the claim language which distinguishes a difference between a first memory and an auxiliary memory. The language 'distinct and separate' does not define the composition or type of memories nor does it provide any details as to the connectivity of the memories. A memory device can have more than one distinct and separate portion dependent upon the addressing used to access the memory device or totally different types of memory devices can be distinct and separate from each other while totally different types of memory devices can be used as contiguous memory using addressing techniques and therefor not be considered distinct and separate. This language has not been detailed in the claims sufficiently to provide distinct claimed subject matter which has been particularly pointed out thereby providing an indefinitely claimed limitation.

11. Claims 1 and 8 claim a second auxiliary memory without claiming a first auxiliary memory. This inhibits a definite interpretation of the claim language as details of the actual composition and relationship of the memory elements is indistinct and not particularly pointed out in the claim language itself.

12. Claims 2 and 9 are considered indefinite as having auxiliary memory with the independent claims claiming a second auxiliary memory without distinctly claiming a first auxiliary memory, however, having a second auxiliary memory strongly implies a first auxiliary memory. Claims 2 and 9 are therefor considered indefinite due to the lack of antecedent basis for the term '*said auxiliary memory*'.

13. Claims 2-7 and 9-11 are indefinite as having the same failings as the claims upon which they depend.

*35 USC § 102*

14. The rejection of claims 1-12 as being anticipated by DeRoo et al. is *maintained* and updated to show the rejection of the claimed amendments.

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by DeRoo et al.

17. DeRoo teaches the invention (claim 1) as claimed including a method for controlling the access to all or part of the content of a first memory integrated with a microprocessor (e.g., see Summary of the Invention, col. 2, lines 27-44) with the first memory being an EEPROM, the method comprising:

executing an access control algorithm contained in a second auxiliary memory using a priority-holding interrupt is taught as capturing writes to a protected range of addresses rather than allowing a signal such as a global erasure to take place with the use of an access control algorithm contained in a second auxiliary memory being inherent as all memory devices or elements have accessing addressing information which is essentially an access control algorithm (e.g., see col. 78, lines 20-36);

accessing the content of the first memory with the access control algorithm using at least one register of keys is taught as a write-once-read-many (WORM) register which is accessed when a cold reboot of the system is performed (e.g., see col. 84, lines 30-47); and,

wherein the second auxiliary memory is distinct and separate from the first memory and the content of the auxiliary memory being programmed only once is taught as the algorithms required which allows an update to the firmware at the time of a cold reboot to the system (e.g., see col. 84, line 30 to col. 85, line 13). The auxiliary memory being distinct and separate from the first memory is clearly taught as several different types of memories are shown in the figures and discussed in the detailed description (e.g., see Figures 22-34 and col. 69, line 10 and col. 85, line 14).

As to claim 2, DeRoo teaches at least one sub-program authorizing the execution of a function of access to the first memory is contained in the auxiliary memory (e.g., see 78, line 21 to col. 79, line 21).

As to claim 3, DeRoo teaches the priority-holding interrupt is non-interruptible even by itself as an HUI trap (e.g., see col. 79, lines 23-36).

As to claim 4, DeRoo teaches the priority-holding interrupt is generated provided that a signal (mode) indicative of an access control operating mode is in an active state as an HUI trap which is generated with a global erase is in an active state (e.g., see col. 79, lines 23-36).

As to claim 5, DeRoo teaches the priority holding interrupt can be generated upon occurrence of an interrupt request coming from the outside of the integrated circuit or from the inside as the interrupt being generated either by software or hardware (e.g., see col. 79, lines 23-36).

As to claim 6, DeRoo teaches the first memory is a program memory containing embarked functions with the embarked functions including functions related to resets of the system under different conditions (e.g., see col. 80, lines 21-44).

As to claim 7, DeRoo teaches the step of accessing the content of the first memory with the access control algorithm using at least one register keys includes using the content of at least one integrated storage element along with the content of the key register with the key register being taught as a write-once-read-many memory register (e.g., see col. 78, lines 20-36).

18. DeRoo teaches the invention (claim 8) as claimed including a circuit comprising:  
a microprocessor integrated with at least a first memory which includes a second auxiliary memory adapted to contain a sub-program enabling authorizing the execution of a function of access to the first memory with the auxiliary memory being programmable only once with the first memory being an EEPROM and the auxiliary memory being a WORM register (e.g., see col. 79, line 23 to col. 85, line 13).

As to claim 9, DeRoo teaches a means for selecting a memory at the input of a memory interface of the microprocessor (e.g., see col. 75, lines 9-47);

the auxiliary memory as a WORM register (e.g., see col. 84, lines 29-47); and,

the first memory, the selection of the first memory otherwise than the execution of a function that it contains, requiring an authorization from an algorithm contained in the auxiliary memory and using the content of at least one integrated storage element and the content of the key register (e.g., see col. 84, line 29 to col. 85, line 13).

As to claim 10, DeRoo teaches the first memory and the storage element are the same program memory (e.g., see col. 75, line 8 to col. 78, line 19).

As to claim 11, DeRoo teaches a means for generating a priority-holding interrupt for executing the sub-program, the generation occurring provided that an HUI trap is needed to prevent a global erase of the protected address range (e.g., see col. 79, lines 23-37);

a signal (mode) indicative of an access-control-operating mode is in an active state with the HUI trap providing a signal mode when the global erase is in an active state (e.g., see col. 79, lines 23-37);

an access to the first memory has been requested otherwise than for a non-interruptible execution of one of the functions that it contains as access to the EEPROM (e.g., see col. 79, lines 23-37); and,

an interrupt signal is active, the resulting priority-holding interrupt being non-interruptible even by itself (e.g., see col. 79, lines 23-37).

### ***Response to Applicant's Remarks***

19. Applicant's arguments filed April 20, 2005 have been fully considered but they are not persuasive.

20. As to the auxiliary memory being distinct from the first memory, this limitation is being argued to a greater extent than supported by the actual claim language. Also, there is not a requirement in the actual claim language that the auxiliary memory cannot also contain program type content. In a system such as the one taught by DeRoo, there are multiple elements and memories used for providing access control of the various memories. Without the claim language being more specific, this limitation is taught to the extent required by the actual claim language.



Art Unit: 2187

---

### ***CONCLUSION***

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on M-TH from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2187, Donald Sparks, can be reached for general questions concerning this application at (571) 272-4201. Additionally, the official fax phone number for the art unit is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.



Reba I. Elmore  
Primary Patent Examiner  
Art Unit 2187

June 13, 2005